CLAIMS

1. (Previously presented) A method of fabricating a CMOS device comprising the steps of:

(a) forming a gate dielectric on a semiconductor substrate that can be sectioned into a p-well region for forming an NMOSFET and a n-well region for creating PMOSFET;

(b) forming an aluminum nitride buffer layer material over the gate dielectric;

(c) depositing a first metal on the buffer layer;

(d) selectively etching the first metal with a first etchant so that the buffer layer is exposed on one of said p-well and n-well regions;

(e) depositing a second metal on both the exposed buffer layer and the remaining first metal;

(f) removing said first metal and said second metal and said buffer layer in selected areas so as to form a PMOSFET gate electrode and an NMOSFET gate electrode of said CMOS device; and

(g) annealing remaining portions of said first metal and said second metal and said buffer layer to consume said portions of said buffer layer by reacting with said first metal and said second metal to form first and second conductive alloys with first and second work functions respectively.

2. (Original) A method as recited in claim 1 wherein said buffer layer material is selected to have a resistance to said first etchant for protecting said gate dielectric from said first etchant.

3. (Cancelled)

4. (Previously presented) A method as recited in claim 1 wherein said buffer layer has a buffer layer thickness less than 20nm.

5. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical solution including a mixture of sulfuric acid and hydrogen peroxide.

6. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical solution including a mixture of hydrofluoric acid and hydrogen peroxide.

7. (Original) A method as recited in claim 1 wherein said annealing is done at a temperature in excess of 400°C.

8. (Original) A method as recited in claim 1 wherein said first metal is hafnium and said second metal is tantalum.

9. (Original) A method as recited in claim 1 wherein said forming a buffer layer material includes a process selected from the group consisting of physical vapor deposition (PVD), chemical vapor deposition (CVD) and atomic layer deposition (ALD).

10. (Previously presented) A method as recited in claim 1 wherein a composition ratio of the aluminum nitride is selected to achieve desired work functions of said metal alloys.

11-13. (Canceled).

14. (Previously presented) A method as recited in claim 1 wherein the first metal and second metal are selected from the group consisting of titanium (Ti), hafnium (Hf) and tantalum (Ta).

15. (Previously presented) A method as recited in claim 1 wherein the first metal and second metal have an electronegativity of less than 1.34.

16. (Previously presented) A metal gate for CMOS applications, wherein the contact area between said metal gate and adjacent metal gate dielectric is comprised of an alloy formed from aluminum nitride and a metal whose electronegativity is less than 1.4.

17. (Original) A metal gate as in Claim 16, where the metal is Hf, and the alloy has a work function of approximately 4.4Ev, appropriate for NMOS.

18. (Original) A metal gate as in Claim 16, where the metal is Ta, and the alloy has a work function of approximately 4.9Ev, appropriate for PMOS.